Tungsten silicide is typically deposited by Chemical Vapor Deposition using WF_6 and either SiH_4 or DCS. Titanium (Ti) and Titanium Nitride (TiN) films are typically deposited by Physical Vapor Deposition (PVD) from a suitable metal target in ultra high vacuum .

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. An optical element consisting of:

   a transparent insulating substrate;

   a circuitry layer on the insulating substrate; and

   an opaque optical shielding layer disposed to lie between the insulating substrate layer and the circuitry layer.

2. The optical element of claim 1, wherein the circuitry layer includes an active polysilicon layer, and the shielding layer is between the insulating substrate and the active polysilicon layer.

3. The optical element of claim 1 wherein the shielding layer comprises a material that

is unaffected by exposure to temperatures up to 1,100 EC

4. The optical element of claim 2 wherein the shielding layer comprises a material that is unaffected by exposure to temperatures up to 1,100 EC

5. The optical element of claim 1 wherein the optical element is part of a liquid crystal display and the opaque shielding layer also functions as a black matrix for said display.

6. A liquid crystal display, comprising:

a first transparent plate having an upper surface;

on said upper surface, an array of opaque optical shielding areas;

on each of said shielding areas, a thin film transistor having a source, a drain, an active region, a gate oxide layer, and a gate pedestal over the gate oxide;

a first dielectric layer that fully covers said thin film transistor, including the gate pedestal;

on the first dielectric layer a wiring layer;

a second dielectric layer that covers the wiring layer;

on the second dielectric layer, additional wiring and dielectric layers, including a topmost dielectric layer;

on the topmost dielectric layer, an array of transparent conductive pixel control elements;

a passivation layer on the topmost dielectric layer and pixel elements;

a second transparent plate having a lower surface;

on said lower surface, a layer of transparent conductive material; and

the transparent plates being aligned to face, and lie parallel to, one another, with a space between them that is filled with liquid crystal material.

7. The liquid crystal display described in claim 6 wherein the opaque shielding layer is selected from the group consisting of a thermally deposited silicon nitride layer, a silicon oxide silicon nitride laminate, and a refractory metal encapsulated in a barrier layer.

8. The liquid crystal display described in claim 6 wherein the opaque shielding layer has a thickness between about 0.05 and 1 microns.

9. The liquid crystal display described in claim 6 wherein said shielding layer further comprise a refractory metal or a metal silicide and, between said first transparent plate and shielding layer, there is, under the shielding layer, a glue layer selected from the group consisting of titanium and titanium nitride.

10. The liquid crystal display described in claim 6 further comprising, between the shielding layer and the thin film transistor, a barrier layer, selected from the group consisting of tungsten nitride, titanium nitride, a laminate of tungsten nitride and silicon oxide, a laminate of tungsten nitride and silicon nitride, a laminate of tungsten nitride and silicon oxynitride, a laminate of titanium nitride and silicon nitride, a laminate of titanium nitride and silicon oxide, and a laminate of titanium nitride and silicon oxynitride.

11. The liquid crystal display described in claim 6 wherein no black matrix element is present and said shielding element also serves to block out light between pixels..

12. The liquid crystal display described in claim 6 wherein the thin film transistor is polysilicon.

13. The liquid crystal display described in claim 6 wherein said display forms part of a digital projection system.

14. The liquid crystal display described in claim 6 wherein the shielding element is a reflective material.

15. The liquid crystal display described in claim 6 wherein the shielding element is a non-reflective material as well as a good thermal conductor and is thermally coupled to a heat sink.

16. A process for manufacturing a liquid crystal display, comprising the sequential steps of:

providing a first transparent plate having an upper surface;

depositing on said upper surface an opaque optical shielding layer and then patterning and etching said shielding layer to form individual shield areas;

forming, on each of said shielding areas, a thin film transistor having a source, a drain, an active region, a gate oxide layer, and a gate pedestal over the gate oxide;

depositing a first dielectric layer to fully cover said thin film transistor, including the gate pedestal;

on the first dielectric layer depositing a metal layer which is then patterned and etched to form a wiring layer;

depositing a second dielectric layer that covers said wiring layer;

on the second dielectric layer, depositing a black matrix layer then patterning and etching said layer to form a black matrix element that is positioned to overlie and overlap the thin film transistor;

on the black matrix and the second dielectric layer, depositing a third dielectric layer;

on the third dielectric layer, depositing a first layer of transparent conductive material and then patterning and etching said first transparent conductive layer to form a pixel control element;

depositing a passivation layer on the third dielectric layer and on said pixel element;

providing a second transparent plate having a lower surface;

on said lower surface, depositing a second layer of transparent conductive material;

aligning the transparent plates to face, and lie parallel to, one another, thereby creating a space between them; and

introducing, and then confining, liquid crystal material in said space.

17. The process described in claim 16 wherein the first transparent plate is selected from

the group consisting of quartz, glass, and sapphire.

18. The process described in claim 16 wherein the opaque shielding layer is selected from the group consisting of tungsten, titanium, tungsten silicide, titanium silicide, and cobalt silicide.

19 The process described in claim 16 wherein the opaque shielding layer is deposited to a thickness between about 0.05 and 1 microns.

20. The process described in claim 16 wherein said shielding layer further comprise a refractory metal or a metal silicide and, between said first transparent plate and shielding layer, depositing, under the shielding layer, a glue layer selected from the group consisting of titanium and titanium nitride.

21. The process described in claim 16 further comprising depositing, between the shielding layer and the thin film transistor, a barrier layer, selected from the group consisting of tungsten nitride, titanium nitride, a laminate of tungsten nitride and silicon oxide, a laminate of tungsten nitride and silicon nitride, a laminate of tungsten nitride and silicon oxynitride, a laminate of titanium nitride and silicon nitride, a laminate of titanium nitride and silicon oxide, and a laminate of titanium nitride and silicon oxynitride.

22. The process described in claim 16 wherein the step of depositing a black matrix layer then patterning and etching said layer to form a black matrix element, is omitted, whereby

said shielding layer will serve as a black matrix.

23. The process described in claim 16 wherein the thin film transistor is polysilicon.